High-Voltage Solar Power Supply in a 'CMOS-MEMS' Process

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***Abstract*—Solar cell arrays are commonly used as a high-voltage power supply for μrobots and have traditionally been made using custom SOI processes. The ability to create solar power supply in a standard CMOS process would be beneficial due to integration with high-quality transistors and multiple interconnect layers on the same substrate for μrobot control circuitry. However, creating a series connection of p-n junctions in a standard CMOS technology is prevented by the fact that the substrate is common to the entire chip. Various different post-fabrication CMOS micromachining processes are discussed in detail and considered for a series solar cell application. I have shown that a metal interconnect-masked CMOS-MEMS process can yield an array of backside-illuminated p-n junctions that are electrically isolated. This process and design results in a 5 mm x 5mm chip with 2000 isolated p-n junctions, that I estimate can provide approximately 4.8 mW at 1012.5 V in full sunlight.**

I. Introduction

Silicon μrobotics has been an exciting area of research for approximately twenty years and has resulted in some very innovative devices. One such work is a three-chip, 10.5 gram, 2.6 μW, 17 mm^3 robot that was able to shuffle a distance of 3mm [1]. Solar cells are often used as an energy source for μrobots and yield approximately 100-200 μW in full-sunlight ($<$1 μW indoors) per mm^2 of p-n junction area. Due to target sizes in the mm^3 to μm^3 range, untethered μrobots are extremely energy constrained. A μrobot platform generally has three main components: energy source, control system, and mechanics for locomotion. As a result, successful μrobot design requires a strong system-level design focus on efficiency in both the electrical and mechanical energy domains.

While thermal, piezoelectric, and electrostatic actuators have all been investigated for MEMS devices, electrostatics is known to be the most energy efficient actuation method [2]. Thus, electrostatic inchworm motors with gap-closing actuators are often used in μrobotics due to their large force, displacement, and efficiency [1], [2]. The force generated by an electrostatic inchworm motor is:

$$F_e = \frac{1}{2}\epsilon V^2 N_g \frac{A}{g^2} \tag{1}$$

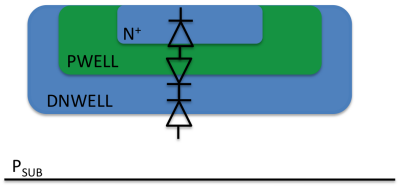
where V is the applied voltage, N_g is the number of gaps, A is the plate area, and g is the gap spacing. Since the electrostatic actuation force is quadratically proportional to the applied voltage, a high-voltage power supply is of paramount importance to generating large electrostatic forces for μrobot locomotion.

II. Background

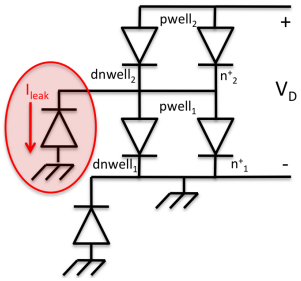
In [1], a custom SOI fabrication process was designed to series connect p-n junctions and create a 50V power supply. While this device worked well for its application, designing in a standard fabrication process is always much preferred. Considering the electronics industry as a whole, standard CMOS fabrication processes are much more ubiquitous than MEMS processes. The ability to create a high-voltage solar power supply in a standard CMOS process would be beneficial due to integration with high-quality transistors and multiple interconnect layers on the same substrate for μrobot control circuitry. However, there are some fundamental problems preventing the realization of such devices.

The main issue in creating a series connection of p-n junctions in a standard CMOS technology is the fact that the substrate (generally p-type) is common to the entire chip. Therefore, any p-n junction formed in the substrate shares a terminal with all others, preventing a series connection. Triple-well CMOS technology is very common today, however, and offers an additional deep nwell (DNWELL) implant to isolate the substrate from surface devices. A triple-well CMOS cross-section is presented in Figure 1a. Shown in the equivalent circuit of Figure 1b, stacking two triple-well cmos structures in series results in a reverse-biased p-n junction (annotated in red) between the shared node and the substrate. This p-n junction is generally more efficient than the series-stacked junctions due to its wider depletion region in the lightly-doped substrate. As a result, the parasitic "leakage" current to ground through this path is greater than the usable photocurrent generated by the stacked devices This forces the output voltage to drop significantly and prevents series solar cell high-voltage generation in triple-well CMOS processes.

In the following sections, the use of a combined 'CMOS-MEMS' fabrication process will be investigated for designing a high-voltage solar power supply. As a hybrid between standard and custom fabrication processes, CMOS-MEMS generally combines the benefits of designing in a standard



(a) Triple-well CMOS process cross-section



(b) Equivalent circuit of two stacked triple-well devices

Fig. 1: Triple-well CMOS fabrication process details

process while requiring much less manual clean room processing than a full custom fab run. This technique could potentially enable the future monolithic integration of power supply, control circuits and MEMS actuators to create a true single-chip μrobot.

III. CMOS-MEMS Process Literature Review

Multiple different methods have been explored for integrating CMOS and MEMS technologies together. In one of these techniques, referred to as 'pre-CMOS', MEMS structures are created on a wafer before entering the standard CMOS fabrication line [3]. One disadvantage to this approach is that the available MEMS processing steps are limited by tight requirements on contaminants for compatibility with the CMOS manufacturing flow. Another fabrication technique, referred to as 'post-CMOS', performs MEMS processing steps after the CMOS fabrication is completed. When using this technique, high temperature processing must be avoided (>400 °C); this has the potential to melt aluminum wiring used in older processes and also change transistor characteristics by mobilizing dopant atoms. Also common today is to perform separate processing of CMOS and MEMS wafers, then hermetically seal the two wafers together to create a vacuum MEMS cavity with interconnects between them. In this paper, a post-CMOS fabrication process which creates MEMS structures in the pre-existing CMOS structure is used. These ideas were pioneered by Gary Fedder at CMU and are often maskless, using the underlying CMOS features as etch stops. Various permutations of this technique will now be discussed in detail.

The use of CMOS interconnect layers as masks for maskless post-CMOS micromachining was first reported in 1996 [4]. First, an anisotropic RIE oxide etch is performed on the finished CMOS wafer. This removes the passivation layer and also removes the inter-layer dielectrics in places where no CMOS metal layer exists. An anisotropic Silicon RIE etch is performed next, which removes the substrate single-crystal Silicon where the dielectrics were etched away in the previous step. The final step in the process is an isotropic Silicon etch that undercuts laterally to create suspended structures. This results in a suspended MEMS structural layer consisting of Aluminum or Copper metal layers sandwiched with CMOS inter-layer dielectrics. This process was used to create a $\approx$ 5 kHz lateral-axis gyroscope with vertical actuation and 0.12 mV/deg/s sensitivity.

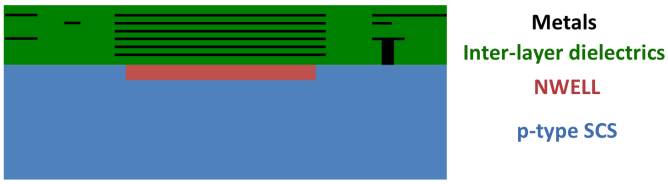
Multiple publications have presented MEMS devices designed incorporating various tweaks of Fedder's original CMOS-MEMS process. One such change presented is to mask the dielectric etch using a photoresist instead of the CMOS interconnect layers [5]. This keeps the top passivation layer intact and prevents floating interconnect layers used for post-processing masks, which could parasitically influence sensitive RF circuits. Another related work overlays vias and passivation etch regions in the CMOS layout to create SCS etch holes through the inter-layer dielectrics, then uses KOH for anisotropic etching along the <111> Silicon direction [6]. While this results in one less post-processing step, creating vias without any metal coverage will likely require CMOS design rule exceptions and may not be approved by the fab. In [7], [8], an initial backside DRIE etch masked by photoresist is used to create a 10-100 μm-thick membrane of single-crystal Silicon. This thin SCS membrane process has been used to design a gyroscope, comb-drive resonator, and z-axis accelerometer.

IV. Analysis

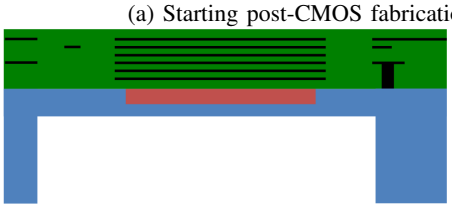
Considering the various CMOS-MEMS process flow discussed in the previous sections, the ideal process steps for creating maximum efficiency, substrate-isolated solar cells will now be presented. A CMOS-MEMS process that uses metal layers for etch masking is selected because it is more compatible with CMOS design rules than [6], without the additional photolithography step required by [5]. In this CMOS-MEMS process flow, single-crystal silicon *must* be covered by metal interconnect to remain after the MEMS etch steps. Since metal will block incident photons, the design must be illuminated from the backside for successful photovoltaic energy harvesting in the SCS p-n junctions. This use case is also advantageous as all of the wiring to connect the solar cells in series is not between the p-n junction and the incident light source.

To optimize solar cell optical-electrical conversion efficiency, the number of free carriers that reach the p-n junction built-in field region should be maximized. The carrier generation rate is much greater near the surface of a semiconductor under incident light, resulting in more free carriers that can be separated by the p-n junction built-in electric field [9]. Thus, it is preferred to have the p-n junction near the surface of the semiconductor. To accomplish this, the initial backside DRIE etch in [7], [8] can be used in combination with backside illumination to bring the p-n junction close to the illuminated

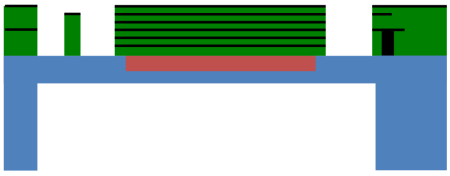
Silicon surface. While this adds an extra step in the post-processing fabrication process, it will lead to a large increase in photovoltaic conversion efficiency. The n-type implant used to create the p-n junction should be the most lightly doped available option, to maximize the depletion region width. The final CMOS-MEMS fabrication process used to create a high-efficiency, high-voltage solar power supply can be seen in Figure 2.



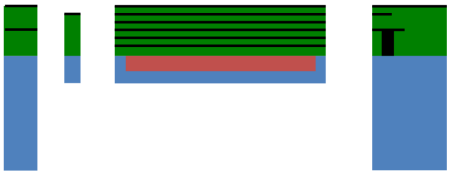
(a) Starting post-CMOS fabrication wafer



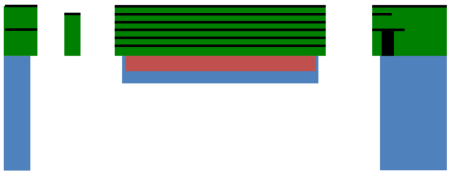
(b) Backside DRIE etch masked by photoresist



(c) Anisotropic CHF_3 / O_2 RIE oxide etch



(d) Anisotropic SF_6 / O_2 RIE Silicon etch



(e) Isotropic SF_6 / O_2 RIE Silicon etch

Fig. 2: CMOS-MEMS Fabrication Process Steps

V. Design

The thickness of the SCS membrane is a very critical parameter in this design, as it drastically effects the free carrier generation rate near the p-n junction. As an estimate, I assume that the n-type implant goes to a depth of approximately 1 μm. Using standard doping levels for this p-n interface the depletion width can be calculated using:

$$W_j = \sqrt{\frac{2\epsilon}{q} V_0 (\frac{1}{N_A} + \frac{1}{N_D})} \quad (2)$$

to be approximately 0.8 μm. The minority carrier diffusion length in single-crystal Silicon is approximately 100-300 μm [10]. Thus, the ideal SCS thickness would be approximately: $1\mu m + 0.8\mu m + 300\mu m \approx 300\mu m$. Reference [8] states that they were able to make the SCS membrane as thin as 10 μm. While they don't state the limiting factors in making it thinner, I suspect their may be issues with etch uniformity and loading across the large areas required for my application. Thus, this etch would be something to test experimentally, targeting a minimum thickness of 300 μm.

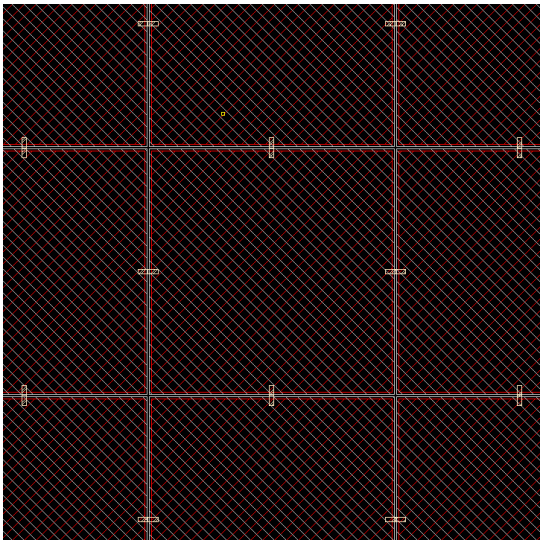
Two other dimensions in the design must also be selected based on the processing steps. The spacing between isolated solar cell islands should be chosen intelligently to maximize the total active area on the chip. Making a conservative estimate of the SCS thickness to be 10 μm, and 10:1 RIE etch anisotropy, the solar cells can be spaced 1 μm apart, defined by the CMOS metal interconnect layer. For structural support, the PV cells should be connected to eachother by the dielectric and metal stack. The width of this bridge must be undercut completely by the isotropic SCS etch to result in electrically isolated solar cell islands. However, a longer isotropic SCS etch also undercuts into the solar cell active area. Thus, this bridge should be made as thin as possible while maintaining structural integrity. I chose a bridge with of 2 μm as this is a common minimum width for MEMS structures. I believe the structural integrity will be sufficient since all p-n junction islands are connected to each neighbor through short bridges, resulting in the stress being distributed over the whole chip area.

VI. Results

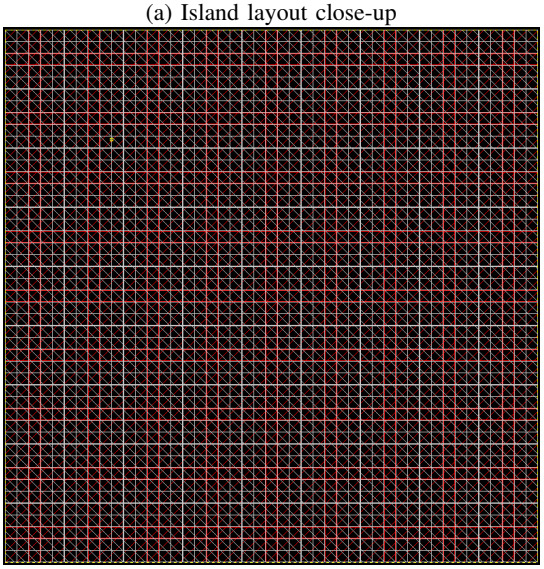
Using the geometric parameters defined in Section V, I created the layout of a 5 mm x 5 mm array of 2000 series solar cells. The drawn layout can be seen in Figure 3. To visualize what the entire structure will look like in three dimensions after CMOS fabrication and post-processing, I constructed a CAD model of the whole array. The CAD model can be seen in Figure 4. The maximum voltage between adjacent solar cell islands is 45V V_{diode} = 0.5V. Considering the Pashcen curve for air at atmospheric pressure, the minimum breakdown voltage is approximately 250V; thus, breakdown will not occur in this design. This 45 x 45 array of solar cells produces an output voltage of 1012.5V at V_{diode} = 0.5V. My analysis and design results in a total active p-n junction area that is approximately 96% of the entire chip area, and will yield approximately 4.8 mW in full sunlight (assuming 20 % solar cell conversion efficiency).

VII. Conclusion

In this report, I have discussed many aspects of high-voltage solar power source design for μrobot applications. The problems with creating a system like this in standard CMOS with triple-well isolation have been presented. Various different post-fabrication CMOS micromachining processes were researched. I have shown that a metal interconnect-masked CMOS-MEMS process can yield an array of backside-



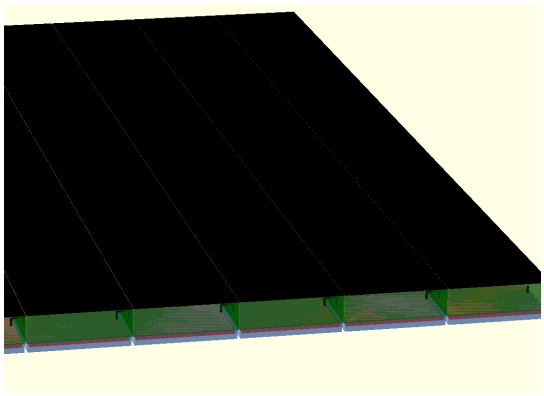
(a) Island layout close-up



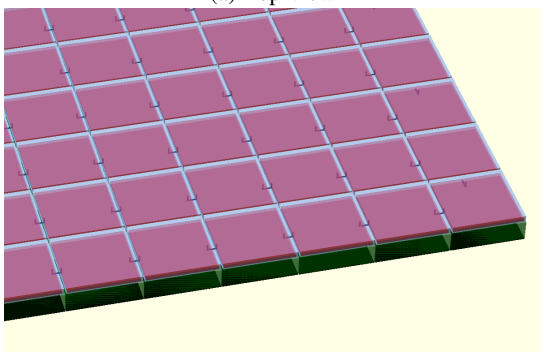
(b) Full 2000 cell array layout

Fig. 3: CMOS layout; grey = metal6, red = NWELL, tan = metal5, orange = via

illuminated p-n junctions that are electrically isolated and can subsequently be connected in series. Performing a back-side DRIE etch step to create a thin single-crystal Silicon membrane can drastically improve the solar cell conversion efficiency, due to their increased proximity to the illuminated semiconductor surface. This process and design results in a 5 mm x 5mm chip with 2000 isolated p-n junctions, that I estimate can provide approximately 4.8 mW at 1012.5 V in full sunlight. Creating a μrobot power supply using this process is also very advantageous, due to potential use of high-quality CMOS transistors to design control circuitry, as well as actuators for locomotion.



(a) Top view



(b) Backside view

Fig. 4: 3-D CAD Model; blue = SCS, red = NWELL, black = metal, green = dielectric

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