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EE230M NMOSFET Design Project Report

1. Design Procedure

To begin our design procedure, we created a MATLAB model based on the long-channel MOSFET equations learned in class. The main equations that this model uses to calculate V_t and I_{off} are shown below:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

$$S \equiv \frac{kT}{q}\ln(10)(1+\frac{C_{dep,\min}}{C_{oxe}})$$

$$I_{off} = I_t 10^{-\frac{V_t}{S}}$$

Our goal in creating this model was to converge towards parameters for a working device, without running many simulations in Sentaurus. Using this model, we estimated I_{off} and V_t, and compared the results to those from Sentaurus for the default device parameters: X_j = 0.01 µm, N_A = 1e18 cm^{-3}, and L_{sp} = 0.02 µm. This comparison showed that our long-channel MATLAB model results were very different from simulation. See Figure 1, where the red diamonds represent the values of V_t and I_{off} from Sentaurus. The higher V_t value predicted by MATLAB is evidence of the short channel effects that are not considered in our model. Differences in the definitions of V_t ($\phi_S = 2\phi_F$ in MATLAB vs. constant current level in simulation) could also account for some of the differences in I_{off} between modeling & simulation.

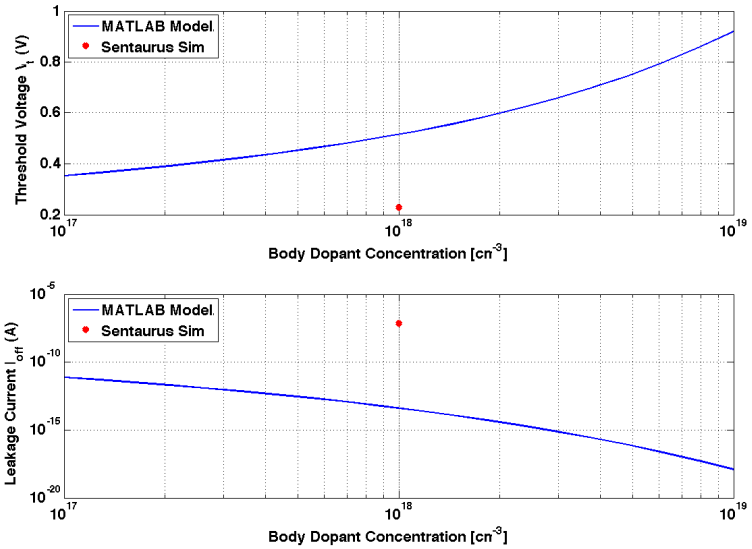

Figure 1: Long-channel MATLAB model vs. Sentaurus sim @ default parameters

After realizing that our long-channel MATLAB model's predictions were quite inaccurate, and analytically modeling short-channel effects would be very difficult, we changed our design approach. Next, we began to investigate the sensitivity of $I_{on,sat}$ and I_{off} to changes in X_j, L_{sp}, and N_A using the simulator. The results of this analysis are shown in Figure 2. In these simulations, one parameter was swept while the other two remained constant at their default value. Thus, this data shows the sensitivities of I_{on} & I_{off} to X_j, L_{sp}, and N_A around the default device parameter values.

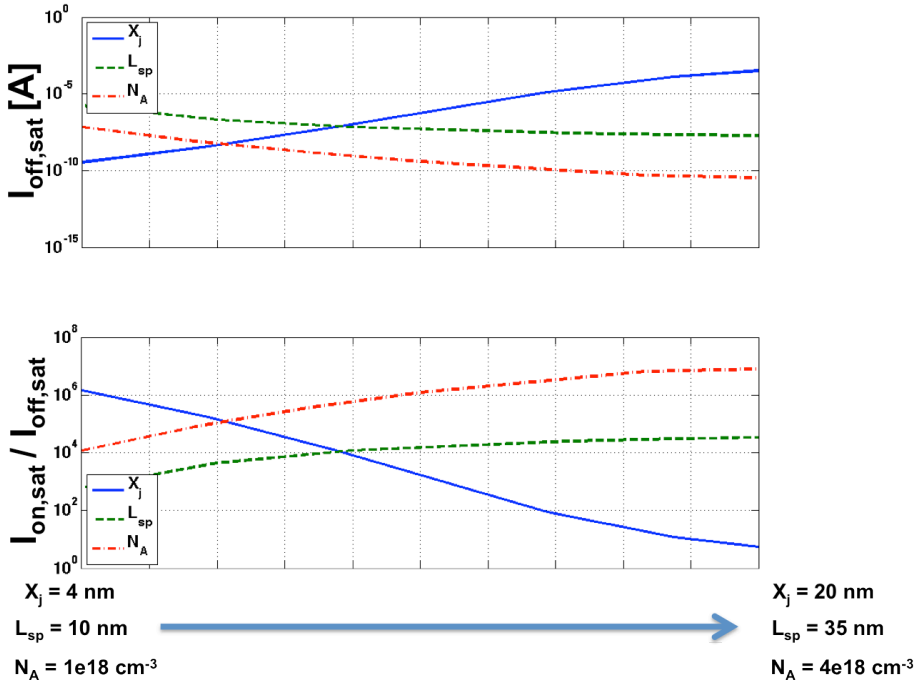

Figure 2: Simulated sensitivity analysis around default parameters

Considering Figure 2, it can be seen that the minimum leakage current is achieved by increasing the channel doping to the maximum allowed concentration. It is also evident that increasing the channel doping can yield the highest I_{on} to I_{off} ratio. Since the initial device parameters meet the I_{on} spec, our goal was to lower I_{off}. However, with N_A = 4e18 cm^{-3}, the I_{off} value still larger than the specification. Thus, other device parameters would need to be changed as well.

Again looking at the curves in Figure 2, it is apparent that the device currents are more sensitive to X_j than L_{sp}. For this reason, we chose to adjust the SDE junction depth and the channel doping simultaneously. Decreasing X_j with N_A = 4e18 cm^{-3}, we were unable to meet both the I_{on} and I_{off} specifications simultaneously. To reach our final working device configuration, we converged to a channel doping of N_A = 2.6e18 cm^{-3}, and a junction depth X_j = 0.005 µm. An illustration of the final NMOS structure is shown in Figure 3.

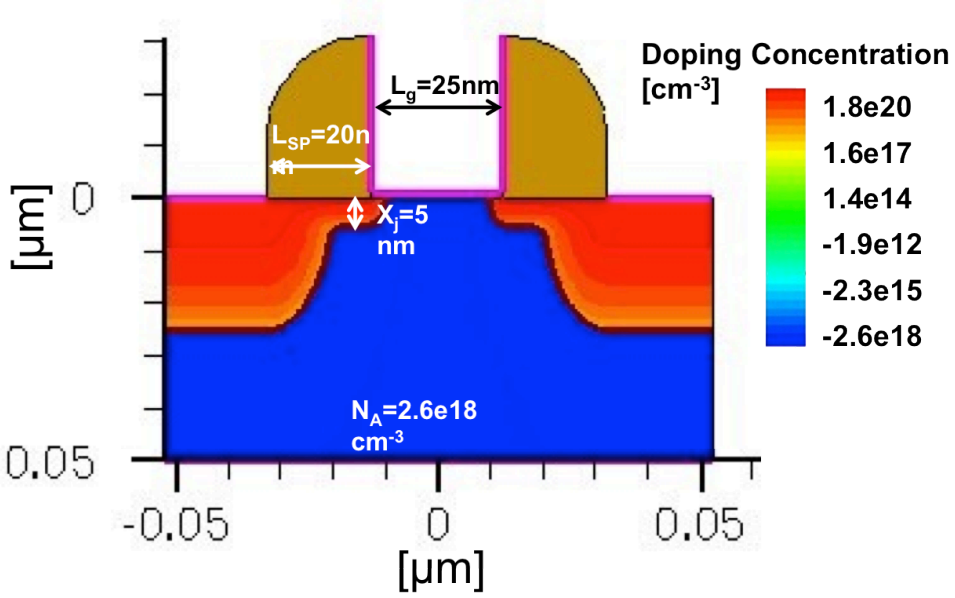

Figure 3: Final NMOS design illustration

2. I_{DS} vs. V_{GS}

All of the following device performance metrics were extracted automatically by Sentaurus, except for the sub-threshold slope which was measured using cursors in the Sentaurus Inspector tool.

N_A [cm^{-3}]	X_J [µm]	L_{SP} [µm]	I_{on} [µA/µm]	I_{OFF} [µA/µm]	S [mV/dec]	DIBL [mV/V]
2.6e18	0.005	0.02	222.3	5.34e-6	83.3	96

Table 1: MOSFET design and performance parameters

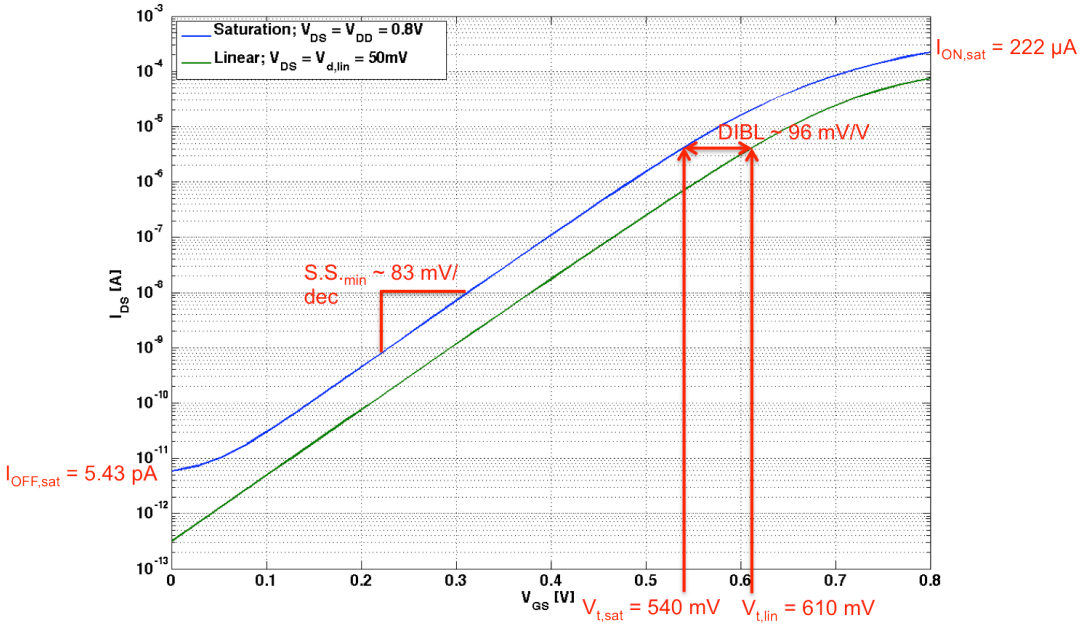

Figure 4: I_{DS} vs. V_{GS} curves for linear and saturation regions

The flatting of the I_{DS} vs V_{GS} curve in saturation near V_{GS} = 0V is due to band-band tunneling at the drain-body junction. Since the channel doping is high, both sides of the drain P-N junction are degenerate, and the depletion width is very small. The narrow depletion region leads to band-band tunneling at large reverse-bias (high V_{DS}).

3. $V_{t,sat}$ vs. L_G

Considering Figure 5, the short-channel effect (SCE) is certainly apparent – the threshold voltage decreases significantly at short gate lengths. This dependence can be modeled by the following equation:

$$\left|V_T\right| - \left|V_{T(long-channel)}\right| \equiv \Delta V_T = \frac{-qN_A W_T}{C_{oxe}} \frac{r_j}{L}\left(\sqrt{1+\frac{2W_T}{r_j}} - 1\right)$$

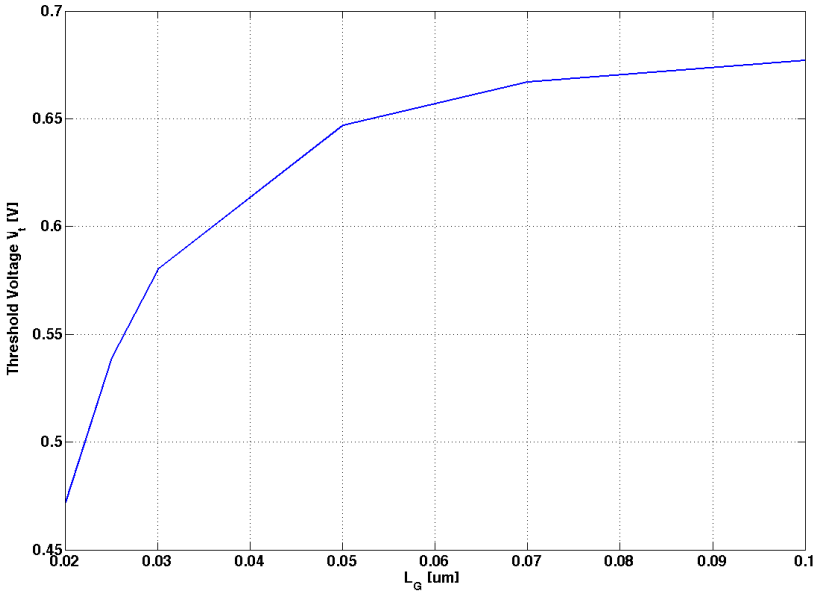

Figure 5: SCE Investigation - $V_{t,sat}$ vs. L_G

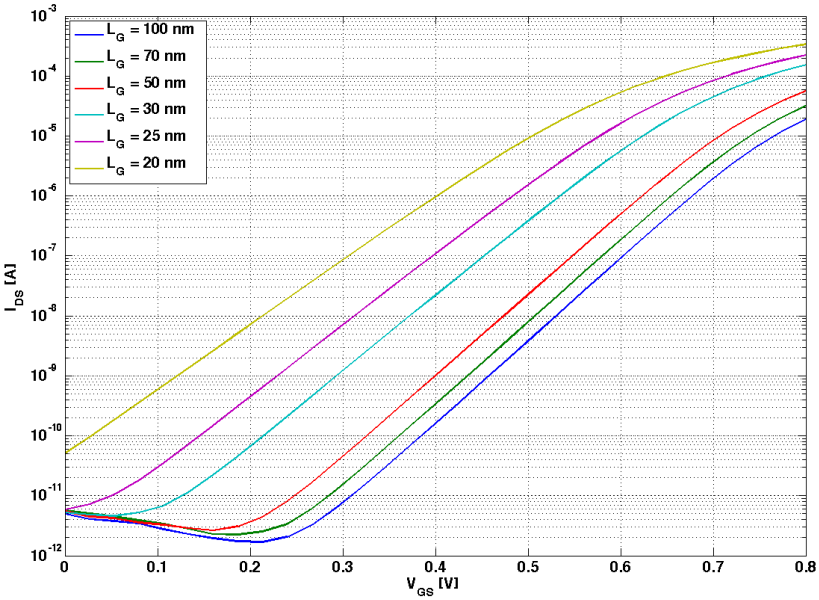

Figure 6: I_{DS} vs. V_{GS} for multiple L_G

The effects of sweeping the channel doping on V_t & I_{off} are compared between our initial long-channel MATLAB model, and the Sentaurus simulator in Figure 7. The difference between these curves can be attributed to V_t roll-off, SCE and DIBL.

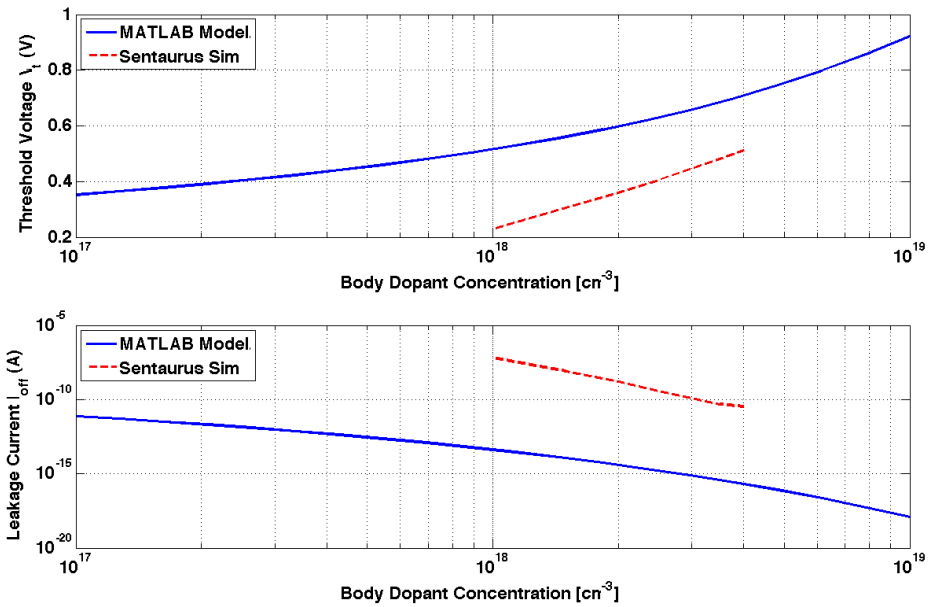

Figure 7: MATLAB model, Sentaurus V_t & I_{off} vs. N_A comparison

4. I_{DS} vs. V_{DS}

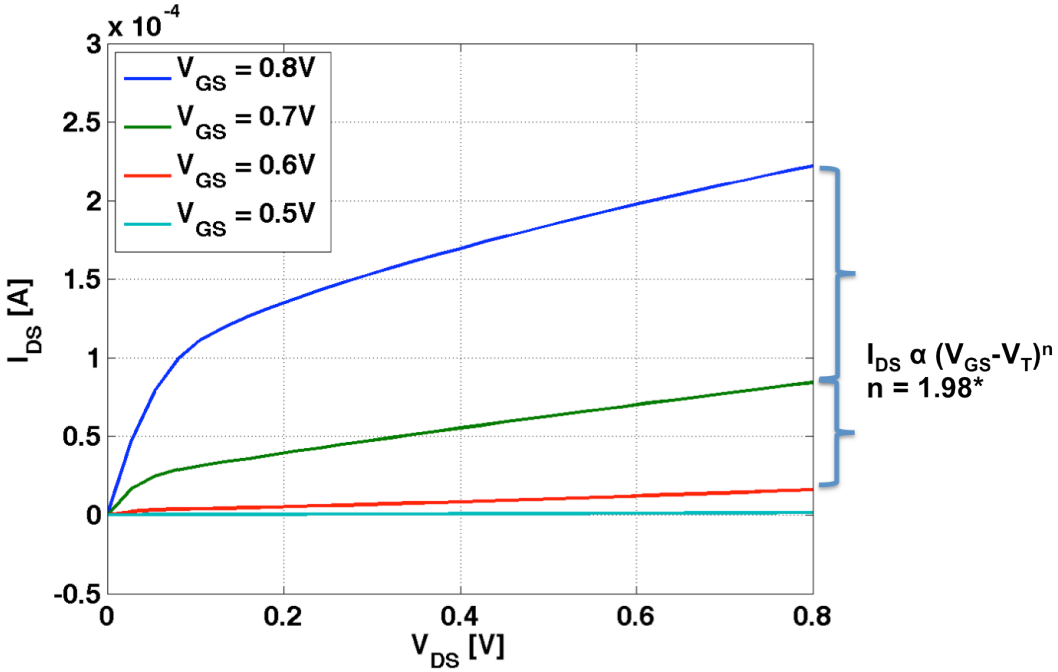

Figure 8: I_{DS} vs. V_{DS} curves

To examine the exponential dependence of saturation current on overdrive voltage, we plotted log(I_{DS}) vs. log (V_{GS}-V_T), shown in Figure 9, and calculated the slope. We found, surprisingly, that our device exhibits a square-law behavior. We believe this is due to our high channel doping. This makes the channel region have a lower mobility, and also a higher threshold voltage. Thus, a higher lateral electric field is required to bring the device into velocity saturation and our device is dominated by the pinch-off effect.

$$I_{DS} \alpha \left(V_{GS} - V_t \right)^n$$
$$n = 1.98$$

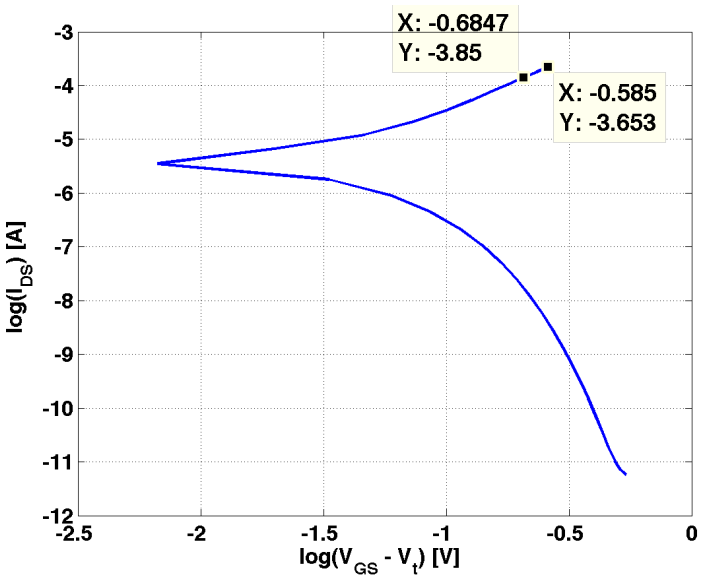

Figure 9: log(I_{DS}) vs. log (V_{DS}) to determine power law dependence

5. Final Remarks

In conclusion, we were able to design a 25nm NMOS device that meets the project specifications: I_{on} > 200 uA/μm & I_{off} < 10 pA/μm. In the process, we learned a lot about the challenges and tradeoffs in short-channel MOSFET design. We also learned how to use an industry-standard software tool for semiconductor device design. These skills will be valuable for potential future coursework in devices, and important for future interactions with device designers in the semiconductor industry.